austriamicrosystems AG

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ams AG

The technical content of this austriamicrosystems datasheet is still valid.

Contact information:

Headquarters:
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

AS1364

1A Low Dropout Linear Voltage Regulator

1 General Description

The AS1364 is a low-dropout linear regulator (LDO) designed to operate from 2V to 5.5V input, that delivers a wide range of highly accurate (±0.75%) factory-trimmed output voltages as well as adjustable output voltages (using an external resistor-divider network).

The ultra-low dropout device requires only 140mV dropout voltage while delivering a guaranteed 1A load current and is therefore perfectly suited for battery-operated portable applications.

Additionally the AS1364 offers extremely low 10µVRMS (100Hz to 100kHz) or 45µVRMS (10Hz to 1MHz) output voltage noise.

Table 1. Standard Products

Model	Output Type	BYP	SET
AS1364-AD	Adjustable	No	Yes
AS1364-_ _	Fixed	Yes	No

The device features an internal PMOS pass transistor (for a low supply current of only 35µA), reset output, a low-power shutdown mode, and protection from short-circuit and thermal-overload conditions.

When in shutdown, a 5kΩ (typ) discharge path is connected between the output pin and ground. The AS1364 is available in a 8-pin TDFN 3x3mm package.

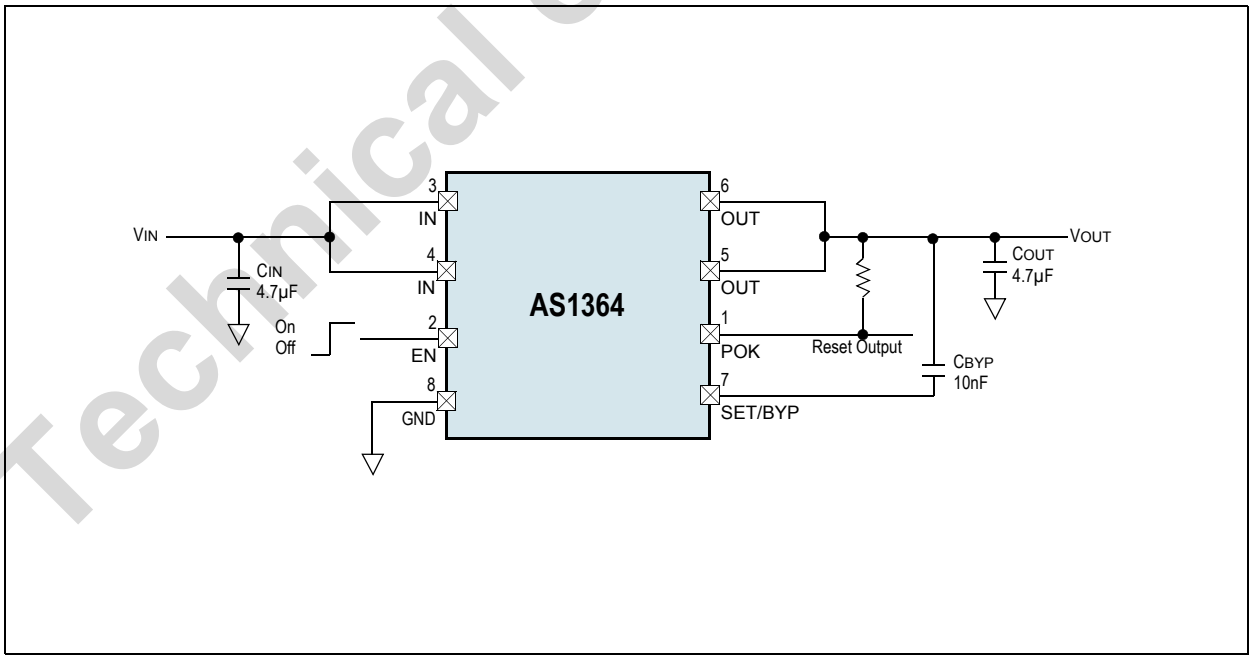
2 Key Features

- Guaranteed Output Current: 1A
- Low Dropout: 140mV @ 1A
- Output Voltage Accuracy: Up to ±0.75%
- 2.0V to 5.5V Input Voltage
- Fixed VOUT: 1.2V to 5.0V
- Adjustable VOUT: 1.2V to 5.3V
- Low Ground Current: 35µA
- Low Shutdown Current: 10nA
- Low Output Noise: 45µVRMS (from 10Hz to 1MHz)
- Thermal Overload Protection
- Output Current Limit
- Output discharge path during shutdown
- 8-pin TDFN 3x3mm Package

3 Applications

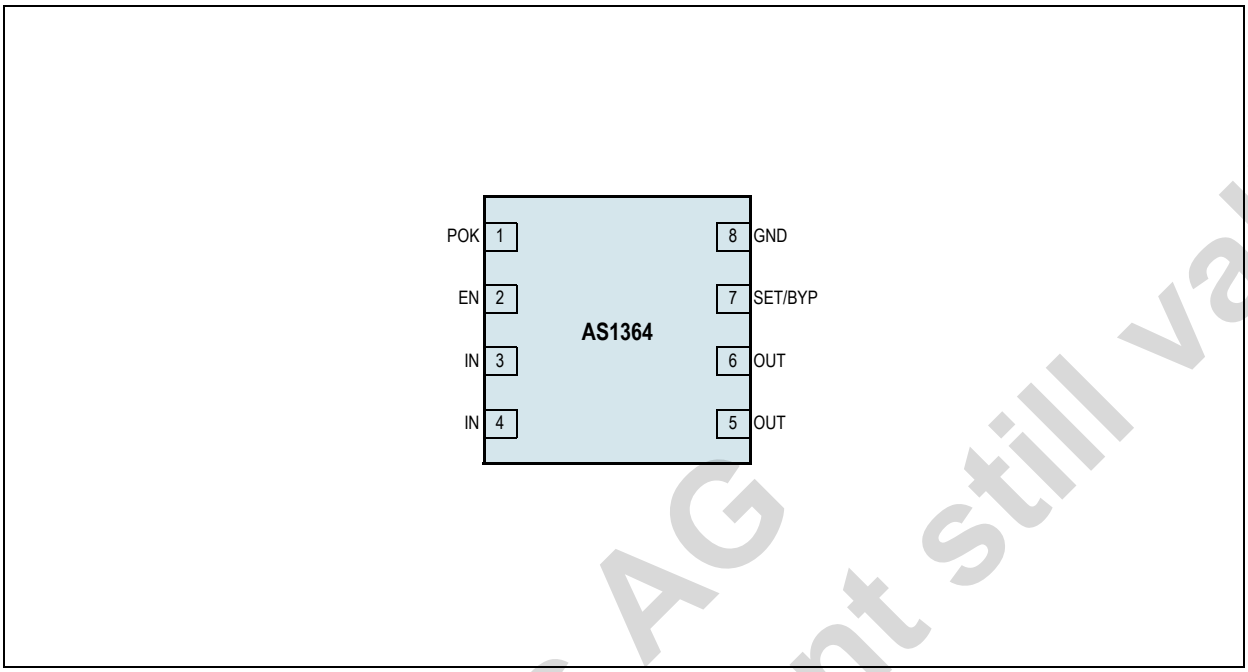
The device is ideal for laptops, PDAs, portable audio devices, mobile phones, cordless phones, and any other battery-operated portable device.

Figure 1. AS1364 - Typical Application Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	POK	**Note: Open-Drain POK Output**. POK remains low while VOUT is below the POK threshold. Connect a 100kΩ pull-up resistor from this pin to OUT to obtain an output voltage (see Figure 1).
2	EN	**Active-Low Shutdown Input**. A logic low disables the output and reduces the supply current to 0.1µA. In shutdown, the POK output is low and OUT high impedance. VDD: Normal operation. GND: Shutdown.
3, 4	IN	**2.0V to 5.5V Supply Voltage.** Bypass with a 4.7µF input capacitor to GND (see Dropout Voltage on page 11). These inputs are internally connected, but they also must be externally connected for proper operation.
5, 6	OUT	**Regulator Output**. Bypass with a 4.7µF low-ESR output capacitor to GND. Connect the OUT pins together externally.
7	SET/BYP	**Voltage-Setting Input**. Connect to GND to select the factory-preset output voltage. Connect this pin to an external resistor-divider for adjustable-output operation (see Figure 1) – (AS1364-AD only) **Bypass Pin**. Connect a 10nF capacitor from this pin to OUT to improve PSRR and noise performance. (AS1364-AD does not offer this feature)
8	GND	**Ground**
Exposed pad	Connect to Substrate	Connect to PCB metal area for heatsink purposes. May be left open or connected to common ground.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
IN, EN, POK to GND	-0.3	+7	V	
OUT, SET/BYP to GND	-0.3	V_{IN} + 0.3	V	
Output Short-Circuit Duration		Infinite		
Latch-Up	-100	+100	mA	*JEDEC 78*
Electrostatic Discharge				
ESD	2		kV	*HBM MIL-Std. 883E 3015.7* methods
Temperature Ranges and Storage Conditions				
Thermal Resistance Θ_{JA}		36.3	°C/W	on PCB
Operating Temperature Range	-40	+85	°C	
Storage Temperature Range	-65	+150	°C	
Junction Temperature		+125	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

Note: All limits are guaranteed. The parameters with min and max values are guaranteed by production tests or SQC (Statistical Quality Control) methods.

V_{IN} = $V_{OUT(NOM)}$ + 500mV or V_{IN} = +2.0V (whichever is greater), C_{IN} = C_{OUT} = 4.7µF, EN = IN, T_{AMB} = -40°C to +85ºC (unless otherwise specified). Typical values are at T_{AMB} = +25ºC.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.0		5.5	V
V_{POR}	Power On Reset	Falling, 100mV hysteresis	1.79	1.87	1.95	V
	Output Voltage Accuracy (Preset Mode)	I_{OUT} = 250mA, T_{AMB} = +25ºC	-0.75		+0.75	%
		I_{OUT} = 250mA	-1.5		+1.5	
		I_{OUT} = 1mA to 1A, V_{IN} > (V_{OUT} + 0.5V)[1]	-2		+2	
V_{OUT}	Adjustable Output Voltage Range		1.2		5.3	V
$V_{SET/BYP}$	SET/BYP Voltage Threshold (Adjustable Mode)	V_{IN} = 2.5V, I_{OUT} = 250mA, V_{OUT} set to 2.0V	1.17	1.20	1.23	V
I_{OUT}	Guaranteed Output Current (RMS)		1			A
I_{LIMIT}	Short-Circuit Current Limit	V_{OUT} = 0	1.1	1.5	2.3	A
	In-Regulation Current Limit	V_{OUT} > 96% of nominal value, $V_{IN} \geq$ 2.0V		1.5		A
	SET/BYP Threshold		50	100	150	mV
I_{SET}	SET/BYP Input Bias Current	$V_{SET/BYP}$ = 1.20V	-100		+100	nA
I_Q	Ground-Pin Current	I_{OUT} = 100µA		35	150	µA
		I_{OUT} = 1A		75	200	
V_{IN} - V_{OUT}	Dropout Voltage [2]	I_{OUT} = 250mA, V_{OUT} = 3.3V		35	85	mV
		I_{OUT} = 1A, V_{OUT} = 3.3V		140	320	
ΔV_{LNR}	Line Regulation	V_{IN} from (V_{OUT} + 100mV) to 5.5V, I_{LOAD} = 5mA	-0.125		+0.125	%/V
ΔV_{LDR}	Load Regulation	I_{OUT} = 1mA to 1A			0.001	%/mA
PSRR	Ripple Rejection	f = 1kHz, I_{OUT} = 10mA, C_{BYP} = 10nF		78		dB
		f = 1kHz, I_{OUT} = 10mA		72		
		f = 10kHz, I_{OUT} = 10mA, C_{BYP} = 10nF		75		
		f = 10kHz, I_{OUT} = 10mA		65		
		f = 100kHz, I_{OUT} = 10mA, C_{BYP} = 10nF		54		
		f = 100kHz, I_{OUT} = 10mA		46		
	Output Voltage Noise	100Hz to 100kHz, C_{OUT} = 3.3µF, C_{BYP} = 10nF;		10		µVRMS
		100Hz to 100kHz, C_{OUT} = 3.3µF;		50		
		10Hz to 1MHz, C_{OUT} = 3.3µF, C_{BYP} = 10nF;		45		
		10Hz to 1MHz, C_{OUT} = 3.3µF;		70		

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Shutdown						
I_{OFF}	Shutdown Supply Current	EN = GND, V_{IN} = 5.5V, T_{AMB} = 25°C		0.01	0.5	µA
		EN = GND, V_{IN} = 5.5V		0.1	15	
V_{IH}	EN Input Threshold	2.0V < V_{IN} < 5.5V	1.6			V
V_{IL}		2.0V < V_{IN} < 5.5V			0.6	V
I_{SHDNN}	EN Input Bias Current	EN = IN or GND, T_{AMB} = +25ºC		1		nA
		T_{AMB} = +85ºC		5		
POK Output						
V_{OL}	POK Output Low Voltage	POK sinking 1mA		0.05	0.25	V
	Operating Voltage Range for Valid POK Signal	POK sinking 100µA	1.1		5.5	V
	POK Output High leakage Current	POK = 5.5V, T_{AMB} = +25ºC		1		nA
		T_{AMB} = +85ºC		5		
	POK Threshold	Rising edge (referenced to $V_{OUT(NOM)}$)	90	94	98	%
Thermal Protection						
T_{SHDNN}	Thermal Shutdown Temperature			170		ºC
ΔT_{SHDNN}	Thermal Shutdown Hysteresis			20		ºC
Output Capacitor						
C_{OUT}	Output Capacitor	Load Capacitor Range	1	4.7		µF
		Load Capacitor ESR			500	mΩ

1. Guaranteed by production test of load regulation and line regulation.
2. Dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 100mV below the value of V_{OUT} measured for V_{IN} = ($V_{OUT(NOM)}$ + 500mV). Since the minimum input voltage is 2.0V, this specification is only valid when $V_{OUT(NOM)}$ > 2.0V.

7 Typical Operating Characteristics

VIN = VOUT(NOM) + 0.5V, CIN = COUT = 4.7µF, TAMB = 25°C (unless otherwise specified).

Figure 3. VDROP vs. IOUT

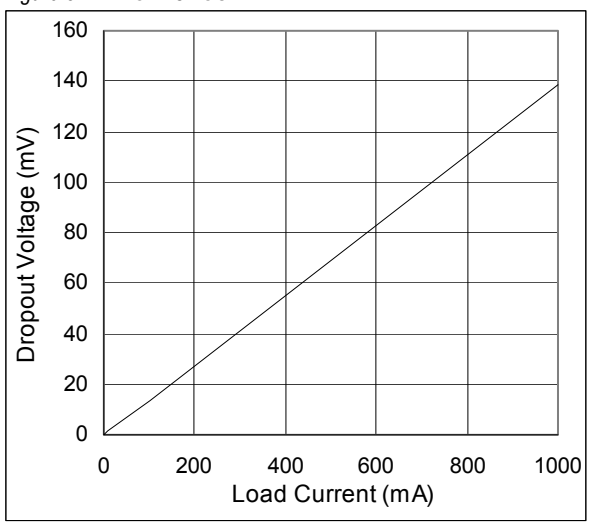


Figure 4. VOUT vs. IOUT; VOUT(NOM) = 3.3V

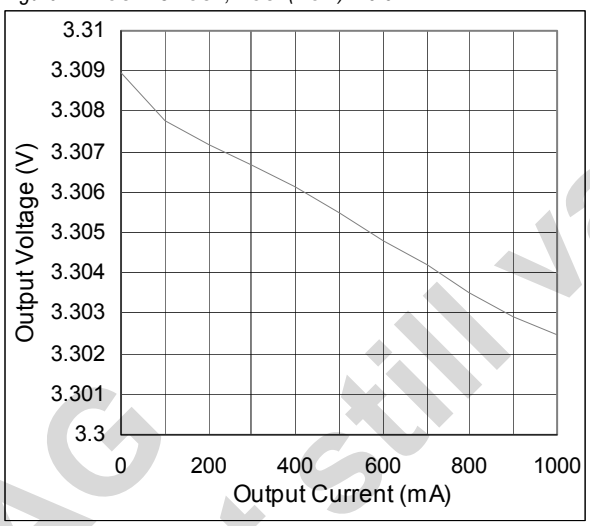


Figure 5. VOUT vs. Temperature; VOUT(NOM) = 3.3V

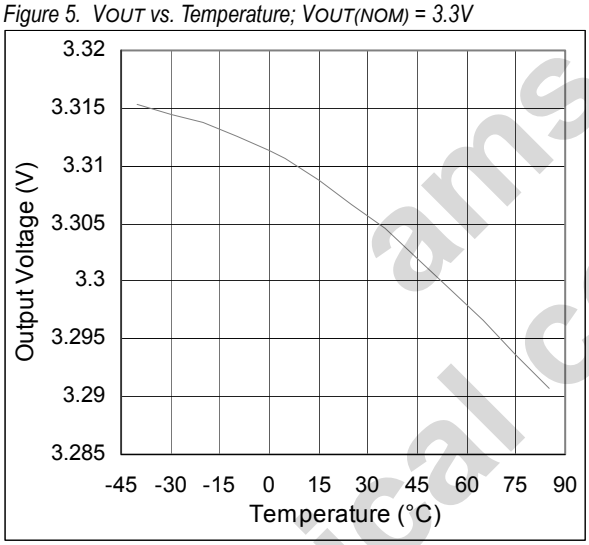


Figure 6. VOUT vs. VIN; VOUT(NOM) = 3.3V

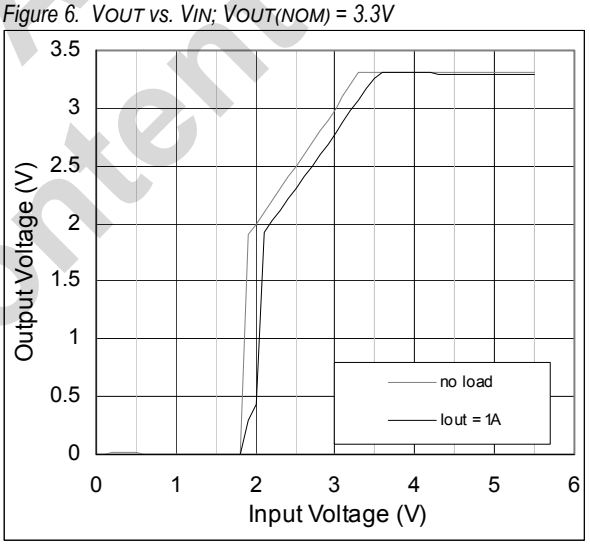


Figure 7. Quiescent Current vs. VIN

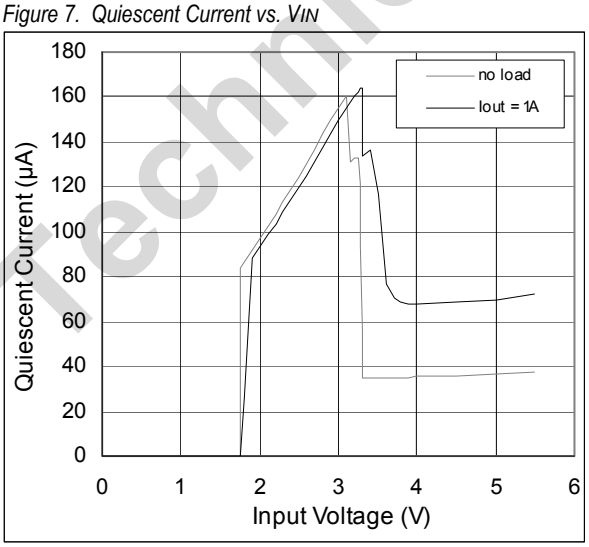


Figure 8. Quiescent Current vs. IOUT

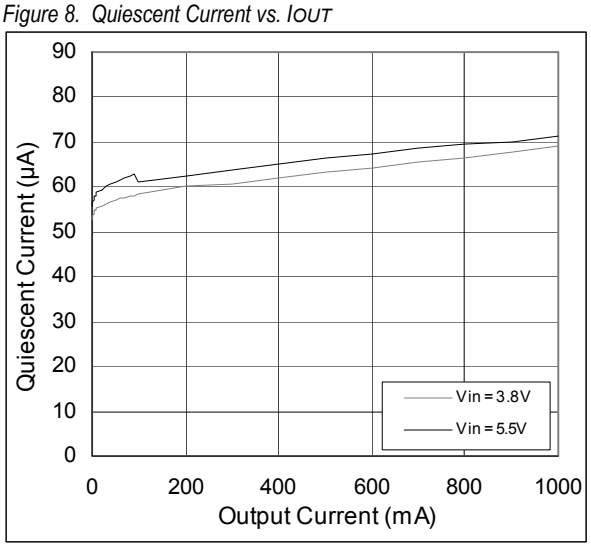


Figure 9. Quiescent Current vs. Temperature

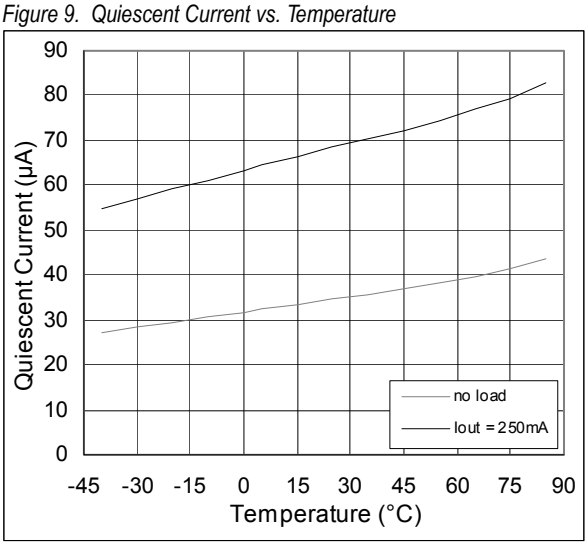


Figure 10. Spectral Noise vs. Freq; I_{OUT} = 10mA

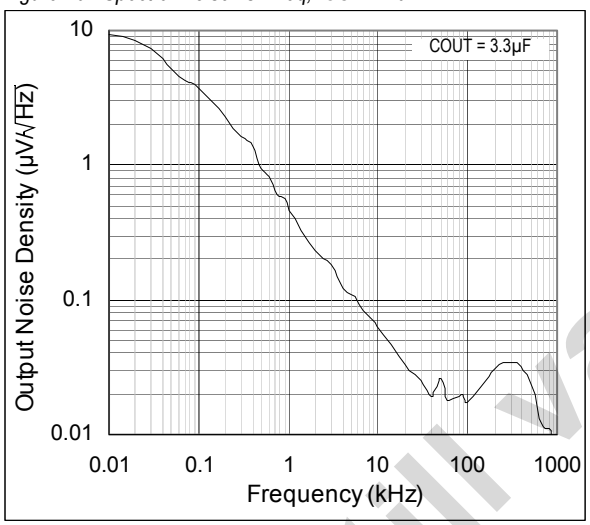


Figure 11. PSRR vs. Frequency; I_{OUT} = 10mA

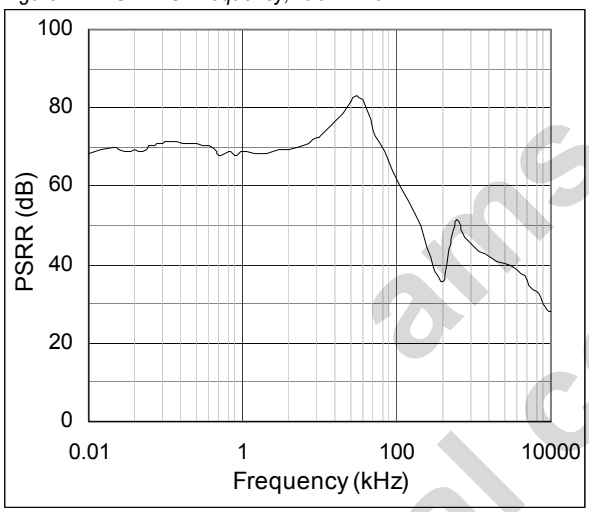


Figure 12. Line Transient Response; V_{IN} = 3.8V to 4.3V, I_{OUT} = 100mA

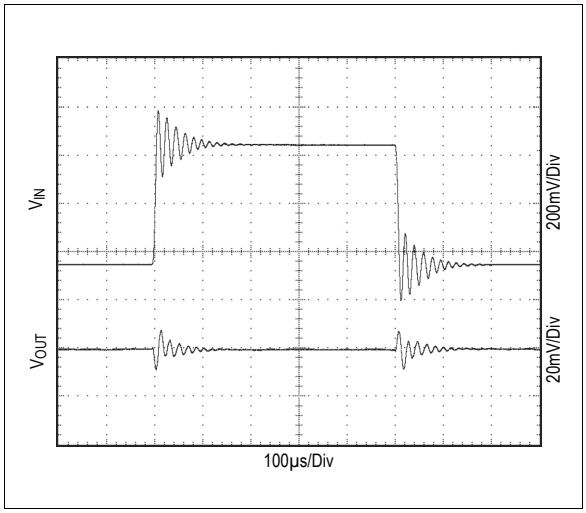


Figure 13. Load Transient Response; V_{IN} = 3.8V, I_{OUT} = 50mA to 500mA

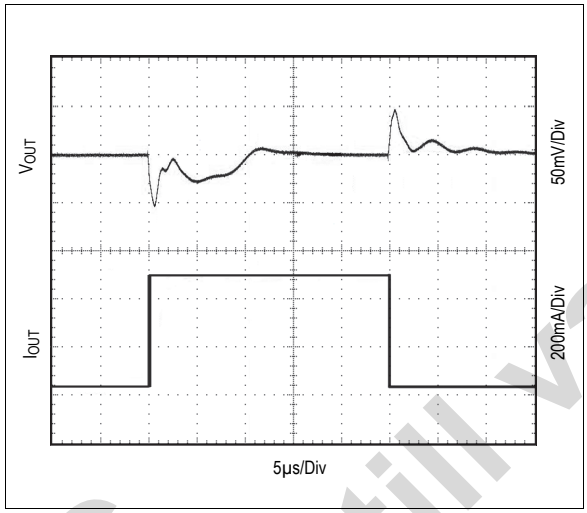


Figure 14. Startup; V_{IN} = 3.8V, I_{OUT} = 100mA

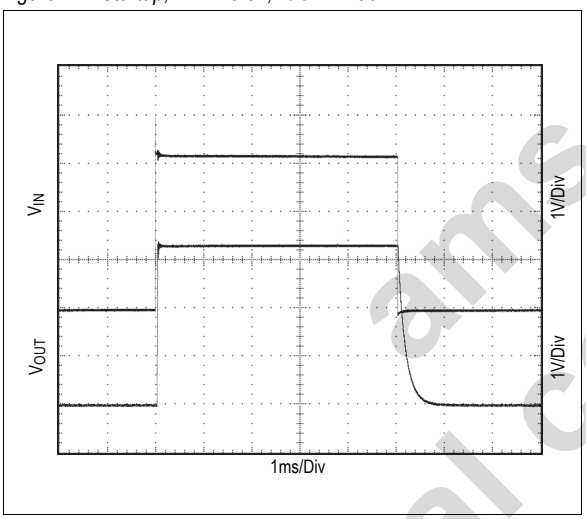
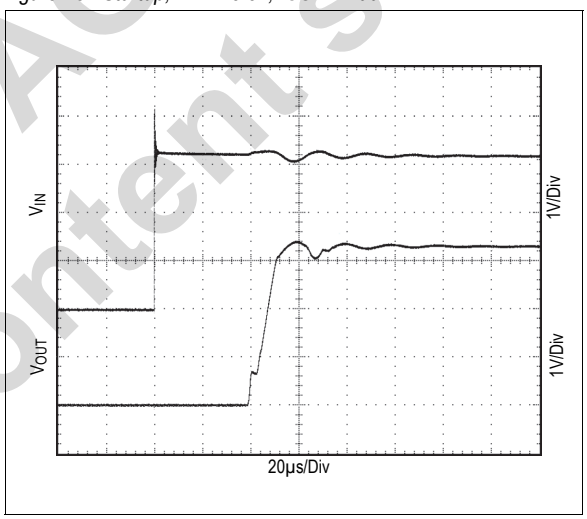


Figure 15. Startup; V_{IN} = 3.8V, I_{OUT} = 100mA



8 Detailed Description

The AS1364 output voltage is factory-trimmed or is adjustable from +1.2V to +5V, and is guaranteed to supply 1A of output current. The device consists of a +1.20V internal reference, error amplifier, MOSFET driver, P-channel pass transistor, internal feedback voltage-divider and a comparator (see Figure 16).

Figure 16. AS1364 - Block Diagram

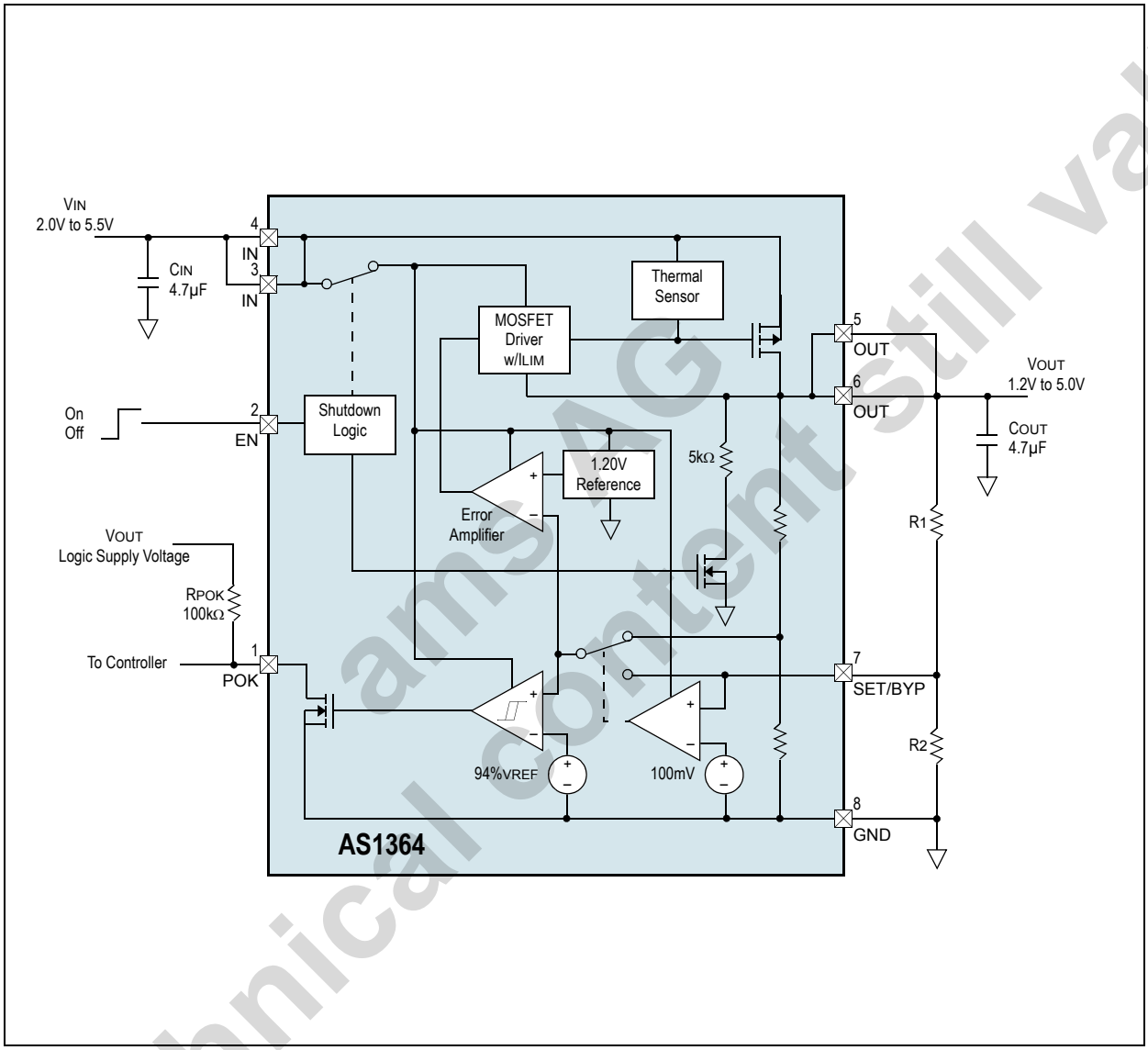


Figure 16 shows the block diagram of the AS1364. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (1.2V REF in Figure 16) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, when additional drive current is required under transient conditions. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

When in shutdown, a 5kΩ discharge path is connected between the output terminal and ground.

8.1 Output Voltage Selection

At the factory trimmed versions of the AS1364 offering the bypass pin (see Figure), the output voltage is then set to an internally trimmed voltage (see Ordering Information on page 18).

For the adjustable AS1364-AD, an output voltage between +1.2V and +5V can be set by using two external resistors (see Figure 17). In this mode, VOUT is determined by:

$$V_{OUT} = V_{SETBYP} \times \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ 1)}$$

Where:
VSET/BYP = 1.2V ±0.03V

A simplification of R1 and R2 selection is:

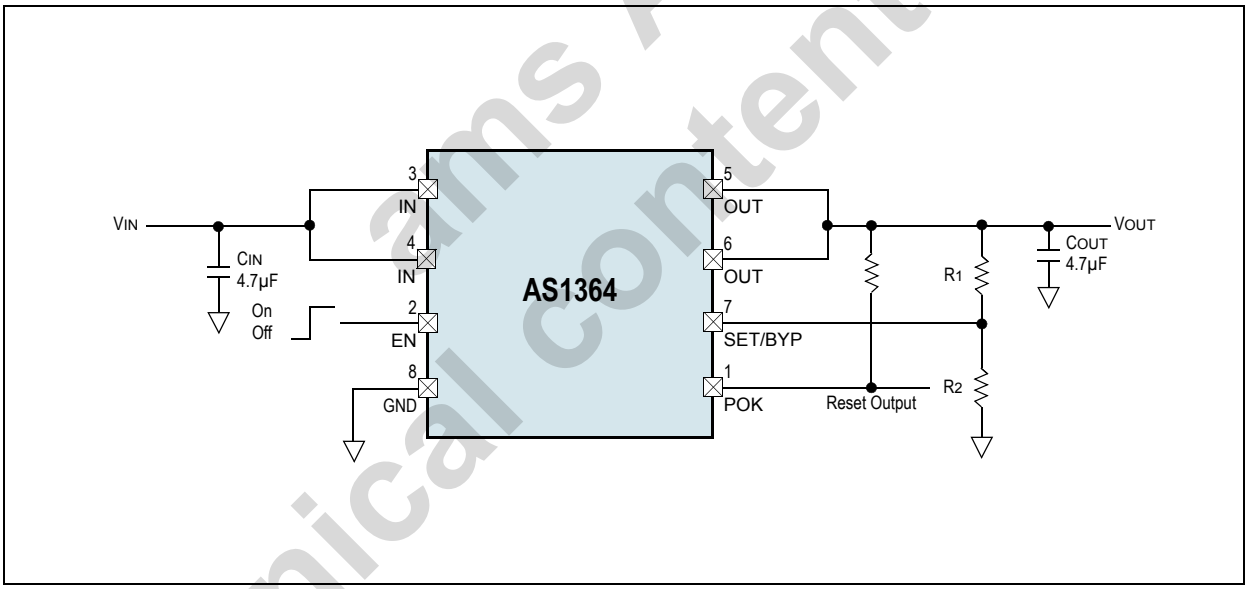
$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{SETBYP}} - 1\right) \quad \text{(EQ 2)}$$

Since the input bias current at SET is less than 100nA, large resistance values can be used for R1 and R2 to minimize power consumption and therefore increasing efficiency.

Note: Up to 125kΩ is acceptable for R2. If the SET pin is connected to GND without a resistor, 3.3V will be set as output voltage.

In preset voltage mode, the impedance from SET to GND should be less than 10kΩ or spurious conditions may cause the voltage at SET to exceed the 50mV threshold.

Figure 17. Adjustable Output Voltage Typical Application



8.2 Shutdown

If pin EN is connected to GND the AS1364 is disabled. In shutdown mode all internal circuits are turned off, reducing supply current to 10nA (typ). For normal device operation pin EN must be connected to IN. During shutdown, POK goes low.

When in shutdown, a 5kΩ (typ) discharge path is connected between the output pin and ground.

8.3 Power-OK

The AS1364 features a power-ok indicator that asserts when the output voltage falls out of regulation. The open-drain POK output goes low when output voltage at OUT falls 6% below its nominal value. A 100kΩ pull-up resistor from POK to a (typically OUT) provides a logic control signal.

POK can be used as a power-on-reset (POR) signal to a microcontroller or can drive an external LED to indicate a power failure condition.

Note: POK is low during shutdown.

9 Application Information

9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \text{(EQ 3)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 18. Graphical Representation of Dropout Voltage

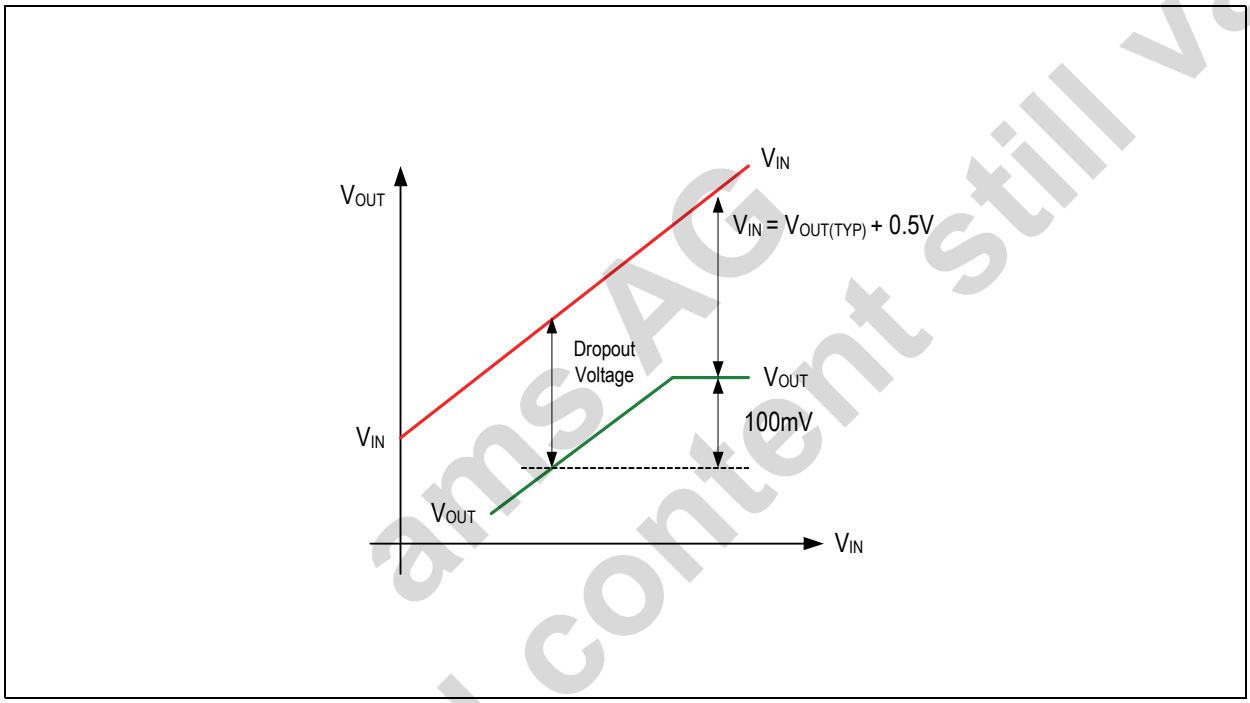


Figure 18 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT-VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

9.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$\textit{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \quad \text{(EQ 4)}$$

Where:
I_Q = Quiescent current of LDO

9.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)}) \ Watts \quad (EQ\ 5)$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)}I_Q \ Watts \quad (EQ\ 6)$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias) \ Watts \quad (EQ\ 7)$$

9.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125ºC (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}ºC/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}ºC/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 19. Package Physical Arrangements

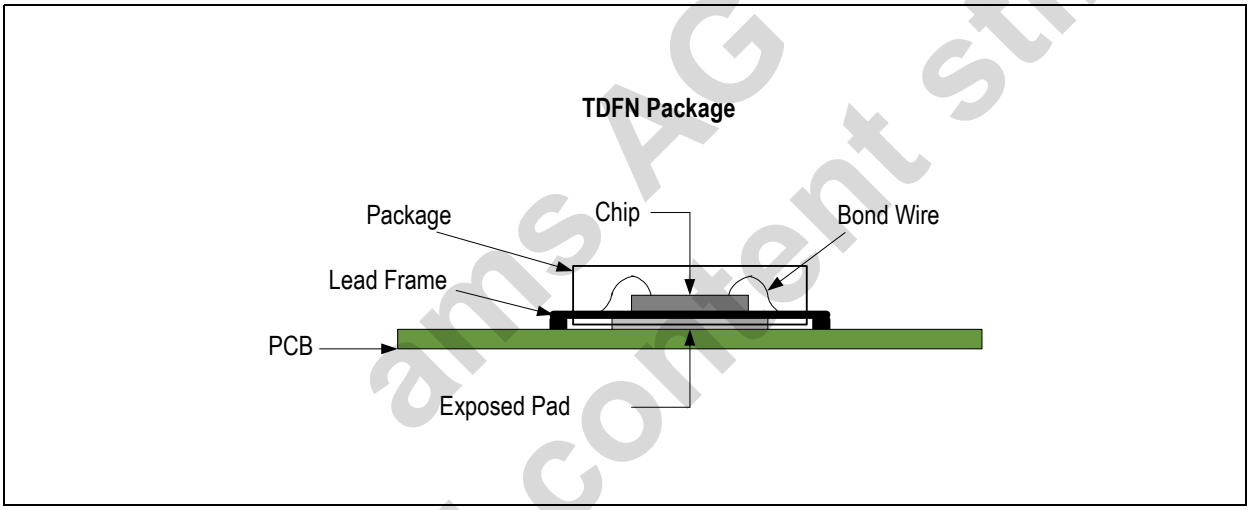
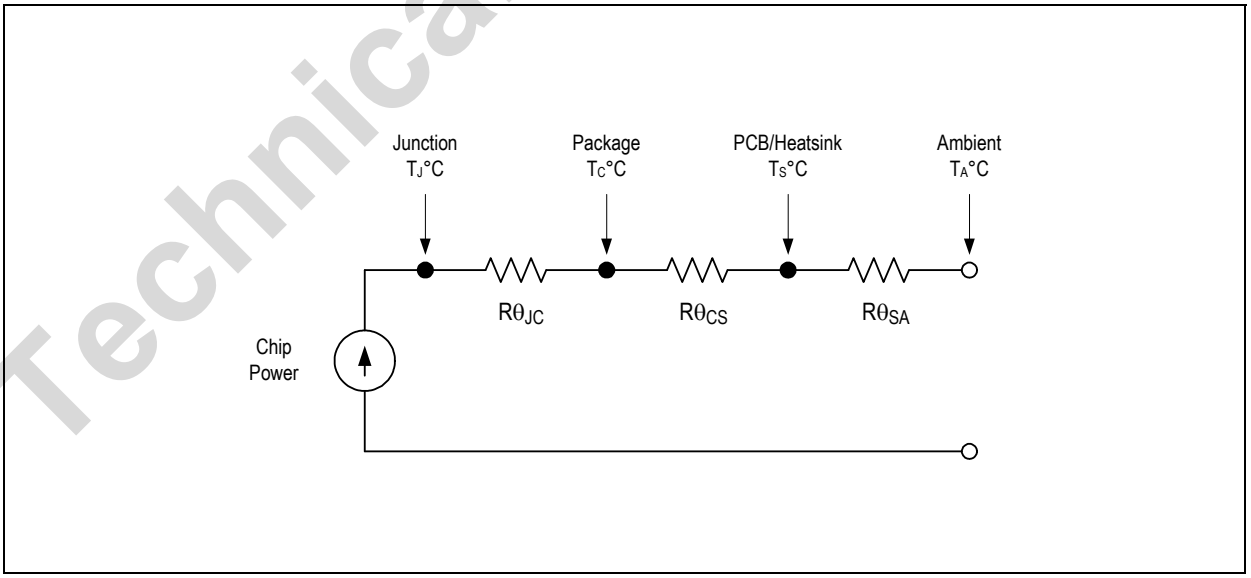


Figure 20. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \text{(EQ 8)}$$

Junction Temperature (T_JºC) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB} \ ºC \quad \text{(EQ 9)}$$

9.5 Explanation of Steady State Specifications

9.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

Line Regulation = $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ and is a pure number

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \ \%/V \quad \text{(EQ 10)}$$

9.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \text{ and is units of ohms } (\Omega) \quad \text{(EQ 11)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \ \%/mA \quad \text{(EQ 12)}$$

9.5.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right) \quad \text{(EQ 13)}$$

The reference tolerance is given both at 25ºC and over the full operating temperature range.

9.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

$$\text{Total \% Accuracy} = \text{Setting \% Accuracy} + \text{Load Regulation \%} + \text{Line Regulation \%} \quad \text{(EQ 14)}$$

9.6 Explanation of Dynamic Specifications

9.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$PSSR = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}} \text{ dB using lower case } \delta \text{ to indicate AC values} \quad \text{(EQ 15)}$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

9.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 4.7µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF max) help to reduce noise and improve load transient-response, stability and power-supply rejection.

9.6.3 Input Capacitor

An input capacitor at VIN is required for stability. It is recommended that a 4.7µF capacitor be connected between the AS1364 power supply input pin VIN and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the VIN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

9.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

9.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \text{Units are Volts, Amps, Ohms.} \quad \text{(EQ 16)}$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}}\right) \quad \text{Units are Volts, Seconds, Farads, Ohms.} \quad \text{(EQ 17)}$$

Where:
C_{LOAD} is output capacitor
T = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

9.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at VIN is stable and within the regulator Min and Max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

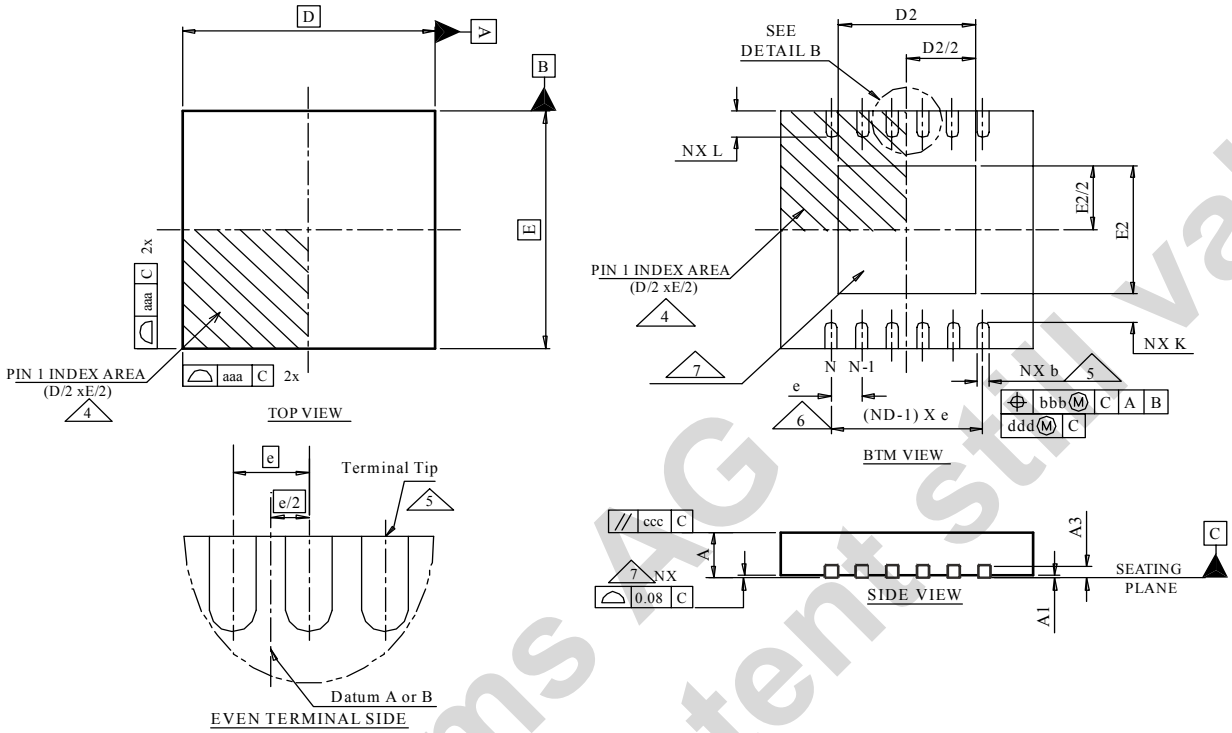
9.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 170ºC (AS1364) threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 20ºC prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

10 Package Drawings and Markings

The device is available in an 8-pin TDFN 3x3mm package.

Figure 21. 8-pin TDFN 3x3mm Package



Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.20 REF		1, 2
L1			0.15	1, 2
L2			0.13	1, 2
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
eee		0.08		1, 2
ggg		0.10		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		3.00		1, 2
E BSC		3.00		1, 2
D2	1.60		2.50	1, 2
E2	1.35		1.75	1, 2
L	0.30	0.40	0.50	1, 2
θ	0°		14°	1, 2
K	0.20			1, 2
b	0.25	0.30	0.35	1, 2, 5
e		0.65		
N		8		1, 2
ND		4		1, 2, 5

Notes:

1. Figure 21 is shown for illustration only.
2. All dimensions are in millimeters; angles in degrees.
3. Dimensioning and tolerancing conform to *ASME Y14.5 M-1994*.
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95-1, SPP-012*. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
7. ND refers to the maximum number of terminals on side D.
8. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

Revision History

Revision	Date	Owner	Description
-	-	-	Initial revisions
1.5	Sep 2011	afe	Changes made across document
1.6	18 Nov, 2011		
1.7	12 Dec, 2011		Updated equations in Power Dissipation section
1.8	03 Apr, 2012		Corrected Figure 1, Figure 16, Figure 17

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The device is available as the standard products shown in Table 5.

Table 5. Ordering Information

Ordering Code	Marking	Output	SET/BYP	Delivery Form	Package
AS1364-BTDT-AD	ASRF	Adjustable (preset to 3.3V)	SET	Tape and Reel	8-pin TDFN 3x3mm
AS1364-BTDT-12*	ASRN	1.2V	BYP	Tape and Reel	8-pin TDFN 3x3mm
AS1364-BTDT-15	ASRG	1.5V	BYP	Tape and Reel	8-pin TDFN 3x3mm
AS1364-BTDT-18	ASRH	1.8V	BYP	Tape and Reel	8-pin TDFN 3x3mm
AS1364-BTDT-30	ASRJ	3.0V	BYP	Tape and Reel	8-pin TDFN 3x3mm
AS1364-BTDT-33	ASRI	3.3V	BYP	Tape and Reel	8-pin TDFN 3x3mm
AS1364-BTDT-45	ASRK	4.5V	BYP	Tape and Reel	8-pin TDFN 3x3mm

*Future product.

Non-standard devices are available between 1.4V and 4.6V in 50mV steps and between 4.6V and 5.0V in 100mV steps. For more information and inquiries contact http://www.austriamicrosystems.com/contact

Note: All products are RoHS compliant.
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austriamicrosystems

Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact